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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/287,304	04/07/1999	AKIRA YAMAMOTO	0941.63012	6149

24978 7590 01/23/2006

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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	**PAPER NUMBER**
2673	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/287,304	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings were received on 21 November 2001. These drawings are acceptable.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. All four independent claims 1 and 14-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claim 1 recites, "a plurality of signal lines that are connected to a plurality of data bus lines via analog switches" (see lines 12-13). Claim 14 recites, "signal lines in each of said blocks are connected to a plurality of data bus lines via analog switches" (see lines 13-14). Claim 15 recites, "divided signal lines in each of said plurality of blocks are connected to a plurality of

data bus lines via analog switches" (see lines 11-13). Claim 16 recites, "a plurality of signal lines that extend into the liquid crystal display device and are connected to a plurality of data bus lines via analog switches" (see lines 10-11).

However, the specification contradictorily teaches the horizontal display signal lines [Fig. 7; 74A] being directly connected to the vertical data bus lines [Fig. 7; 68A], and the display panel [Fig. 7; 16] being connected to the data bus lines [Fig. 7; 68A] via analog switches [Fig. 7; 66] (see Page 8, Lines 7-33 of the instant specification). Although only one inventive embodiment (illustrated in Figure 7) is referenced explicitly here, all other pending embodiments are identical as regarding the aforementioned subject matter.

Due to 'Amendment L' (submitted 31 October 2005), claims 1 and 14-16 also incorporate the new subject matter of *display signals simultaneously being supplied from the plurality of signal lines to the data bus lines and written to the plurality of signal lines from the data bus lines*. This subject matter is argued by the applicants (on page 12, 2nd paragraph of 'Amendment L') as constituting "two-way transmission between the signal lines and the data bus lines." No such *two-way transmission* subject matter has been anywhere described in the instant specification.

5. The remaining claims 2-13 and 17-21 are rejected under 35 U.S.C. 112, first paragraph, due to their respective dependencies upon rejected base claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-6, 8-16, and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima (US 5,654,735).

Regarding claim 1, Nakajima discloses a liquid crystal display device including a data driver [Fig. 1; 13] and a gate driver [Fig. 1; 12], comprising an LCD panel [Fig. 1; 1] having two opposing flat surfaces, an area of one of the flat surfaces for displaying an image, and at least two edges opposing one another about the flat surfaces and outside of the display area; a substrate on which the LCD panel, the data driver and the gate driver are integrally formed; the data driver on a single edge of the at least two opposing edges of the LCD panel being divided into a plurality of blocks [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] so as to divide the LCD panel into sections arranged side by side, which simultaneously supply the LCD panel with display signals respectively supplied thereto, wherein each of the blocks includes a plurality of signal lines [Fig. 1; V_n, V_{n+1}, etc.] that are connected to a plurality of data bus lines [Fig. 1; SIG1-SIG3, $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.], a number of the data bus lines being larger than a number of the signal lines, the display signals simultaneously being supplied from the plurality of signal lines to the data bus lines and written to the plurality of signal lines from the data bus lines, and the blocks are arranged adjacent to each other along the single edge of the LCD panel, and each block includes a series of different signal lines (see Column 4, Line 1 - Column 5, Line 31).

Regarding claim 2, Nakajima discloses a block comprising a shift register [Fig. 1; 15]; signal lines [Fig. 1; V_n, V_{n+1}, etc.] connected to the signal lines and the LCD panel [Fig. 1; 1];

and analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}] provided in the data bus lines and controlled by an output signal [Fig. 1; $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] of the shift register thereto (see Column 4, Lines 1-42).

Regarding claim 3, Nakajima discloses a driver device [Fig. 1; 2] which receives display data [Fig. 1; VIDEO] externally supplied and outputs the display signals derived therefrom to the blocks of the data driver (see Column 4, Line 43 - Column 5, Line 7).

Regarding claim 4, Nakajima discloses a plurality of driver devices [Fig. 1; 21+24, 22+25, 23+26] which are respectively associated with a plurality of ones of the blocks, each of the plurality of driver devices receiving display data [Fig. 1; VIDEO, SIG1-SIG3] externally supplied and outputting the display signals derived therefrom to associated blocks of the data driver (see Column 4, Line 43 - Column 5, Line 7).

Regarding claim 5, Nakajima discloses the display signal lines of the associated blocks have parts extending from one of the plurality of driver devices through a space located between the associated blocks (see Fig. 1).

Regarding claim 6, Nakajima discloses a substrate on which the LCD panel, data driver and gate driver are integrally formed (see Fig. 1; Column 4, Lines 1-42).

Regarding claim 8, Nakajima discloses a display signal supply device [Fig. 1, VIDEO] which outputs the display data to the driver device (see Column 4, Line 43 - Column 5, Line 7).

Regarding claim 9, Nakajima discloses the display signal display device is formed on the LCD panel (see Column 4, Lines 1-42).

Regarding claim 10, Nakajima discloses a display signal supply device [Fig. 1, VIDEO] which outputs the display data to the plurality of driver devices (see Column 4, Line 43 - Column 5, Line 7).

Regarding claim 11, Nakajima discloses each of the plurality of blocks supplies the LCD panel with a given number [three, for instance] of display signals at once (Column 5, Lines 8-31).

Regarding claim 12, Nakajima discloses the driver device comprises a shift register [Fig. 1; 3] which outputs a shift signal [Fig. 1; SH1, SH2, SH3], first latch circuits [Fig. 1; 21-23] which latch the display data in response to the shift signal, and second latch circuits [Fig. 1; 24-26] which latch the display data from the first latch circuits in response to a latch enable signal [Fig. 1; SH4] externally supplied [Fig. 1; SYNC] (Column 4, Line 43 - Column 5, Line 31).

Regarding claim 13, Nakajima discloses digital-to-analog converters [Fig. 3, 202] which convert the display data from the second latch circuits into analog signals (Column 7, Line 60 - Column 8, Line 23).

Regarding claim 14, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Nakajima discloses a liquid crystal display device including a data driver [Fig. 1; 13] and a gate driver [Fig. 1; 12], comprising an LCD panel [Fig. 1; 1] having two opposing flat surfaces, an area of one of the flat surfaces for displaying an image, and at least two edges opposing one another about the flat surfaces and outside of the display area; and groups of signal lines [Fig. 1; V_n, V_{n+1}, etc.] for carrying display signals, the signal lines within each of the groups being adjacent to each other along a single edge of the at least two opposing edges of the LCD panel, and the data driver being divided into a plurality of adjacently arranged blocks [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] from which the groups of signal lines extend over corresponding partial areas of the LCD device so that each of the groups of signal lines is associated with a respective one of the blocks of the data driver, wherein the signal lines in each of the blocks are connected to a plurality of data bus lines [Fig. 1; SIG1-SIG3, $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.], a number of the data bus lines is larger than a number of the signal lines, and the display signals are simultaneously supplied from the groups of signal lines to the data bus lines and written to the groups of signal lines from the data bus lines (see Column 4, Line 1 - Column 5, Line 31).

Regarding claim 15, Nakajima discloses a liquid crystal display device including a data driver [Fig. 1; 13] and a gate driver [Fig. 1; 12], comprising an LCD panel [Fig. 1; 1] having two opposing flat surfaces, an area of one of the flat surfaces for displaying an image, and at least two edges opposing one another about the flat surfaces and outside of the display area; signal lines [Fig. 1; V_n, V_{n+1}, etc.] extending from the data driver and carrying display signals, the data driver and the signal lines being divided into a plurality of blocks [Fig. 1; HSW_n, HSW_{n+1},

HSW_{n+2}, etc.] so that the divided signal lines extending from one of the plurality of blocks extends over a corresponding divided area of the LCD device; wherein the plurality of blocks are adjacent to each other along a single edge of the at least two opposing edges of the LCD panel, the divided signal lines in each of the plurality of blocks are connected to a plurality of data bus lines [Fig. 1; SIG1-SIG3, $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.], a number of the data bus lines being larger than a number of the signal lines, and display signals being simultaneously supplied from the plurality of signal lines to the data bus lines and written to the signal lines to and from the data bus lines (see Column 4, Line 1 - Column 5, Line 31).

Regarding claim 16, Nakajima discloses a liquid crystal display device including a data driver [Fig. 1; 13] and a gate driver [Fig. 1; 12], comprising an LCD panel [Fig. 1; 1] having two opposing flat surfaces, an area of one of the flat surfaces for displaying an image, and at least two edges opposing one another about the flat surfaces and outside of the display area; a substrate on which the LCD panel, the data driver and the gate driver are integrally formed; the data driver being divided into a plurality of blocks [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] arranged side by side along a single edge of the at least two opposing edges of the LCD panel, and each of the blocks has a plurality of signal lines [Fig. 1; V_n, V_{n+1}, etc.] that extend into the liquid crystal display device and are connected to a plurality of data bus lines [Fig. 1; SIG1-SIG3, $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.], a number of the data bus lines being larger than a number of the signal lines, and display signals being simultaneously supplied from the plurality of signal lines to the data bus lines and written to the plurality of signal lines from the data bus lines (see Column 4, Line 1 - Column 5, Line 31).

Regarding claim 18, Nakajima discloses each of the blocks [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] is arranged adjacent to a block of at least one of an immediately preceding block and an immediately following block (see Fig. 1).

Regarding claim 19, this claim is rejected by the reasoning applied in the above rejection of claim 18.

Regarding claim 20, this claim is rejected by the reasoning applied in the above rejection of claim 18.

Regarding claim 21, this claim is rejected by the reasoning applied in the above rejection of claim 18.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima (US 5,654,735).

Regarding claims 7 and 17, Nakajima discloses the use of thin film transistors (see Column 4, Lines 6-7). Yet, Nakajima does not expressly teach the data driver comprising polysilicon transistors. However, the use of polysilicon transistors within data drivers was well known and commonly understood in the art of LCD data electrode driving at the time of invention. Therefore, it would have been obvious to one skilled in the art at the time of invention to use polysilicon transistors within Nakajima's data driver, so as to manufacture the device with commonly available circuitry components.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Response to Arguments

11. Applicants' arguments filed 31 October 2005 have been fully considered but they are not persuasive. The applicants contend the cited prior art of Nakajima (US 5,654,735) neglects teaching what the applicants term, "two-way transmission between the signal lines and the data bus lines." (see Page 12, 2nd Paragraph of the amendment submitted 31 October 2005). However, the examiner respectfully disagrees. As taught by the instant application this so-called *two-way transmission* between the horizontal signal lines [Fig. 7; 74A] and the vertical data bus

lines [Fig. 7; 68] appears to be little more than the inherent result of the signal lines [Fig. 7; 74A] and the data bus lines [Fig. 7; 68] being connected to one another (see Page 8, Lines 7-33 of the instant specification).

In a similar manner, Nakajima clearly discloses display signals simultaneously being supplied from the plurality of signal lines [Fig. 1; V_n, V_{n+1}, etc.] to the data bus lines [Fig. 1; SIG1-SIG3, $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] and written to the plurality of signal lines from the data bus lines, whenever the corresponding analog switch [Fig. 1; HSWn, HSWn+1, HSWn+2, etc.] closes the connection between the signal lines from the data bus lines (see Column 4, Lines 1-42).

In fact, Nakajima's horizontal SIG1-SIG3 lines (see Fig, 1) could be taken for the instant application's plurality of signal lines, and the vertical wiring lines branching off those horizontal SIG1-SIG3 lines could be taken as the instant application's plurality of data bus lines; and yet again it could be said that Nakajima teaches "two-way transmission" (i.e. a connection) between those same signal lines and data bus lines.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

12. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J.P.
11 January 2006

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